10th IEEE Electron Devices Technology
and Manufacturing (EDTM 2026)
Conference

FET100 Speaker

100 YEARS
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IEEE ELECTRON DEVICES SOCIETY

1-4 MARCH, 2026

edtm 2026
Electron Devices Technology and Manufacturing Conference

A Century of Miracles – From the FET's Inception to the Horizons Ahead

From the invention of the FET exactly a century ago to today's ultra-high-performance CMOS, the journey has been propelled by a highly improbable chain of coincidences—a true "mission impossible" that has led to a series of technological miracles. In this talk, we will revisit those extraordinary milestones and explore the next potential miracle that could once again redefine the very limits of performance.

Distinguished Chair
Professor and
Emeritus Professor

Prof. Hiroshi Iwai

國立陽明交通大學
NATIONAL YANG MING CHIAO TUNG UNIVERSITY

Institute of
SCIENCE TOKYO

Hiroshi Iwai is an engineer who has dedicated over 50 years to the development of LSI technologies and products, from the 8 μm PMOS LSI generation in 1973 to the present, through his work at Toshiba Corporation, the Tokyo Institute of Technology / Institute of Science Tokyo, and NCTU / NYCU.

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Developments of GAAFET Technologies and Future Challenges

The transistor has evolved from a theoretical concept to the foundation of modern electronics, driving unprecedented advances in computing power, connectivity, and miniaturization. This talk provides a concise overview of Gate-All-Around (GAA) field-effect transistors, with a focus on Multi-Bridge-Channel FETs (MBCFETs) as the most advanced silicon-based logic architecture for today's scaling challenges.

The evolution from planar MOSFETs, through strain engineering, high-k metal-gate integration, and the FinFET era, to the current inflection point where FinFETs can no longer meet electrostatic control and cell scaling requirements is traced, highlighting key milestones in GAA development from early nanowire concepts to commercial nanosheet-based MBCFETs.

Key aspects of device physics that enable GAA scaling are highlighted, including superior electrostatic control, natural-length reduction, quantum confinement driven transport, and improved mobility across stacked nanosheet geometries. Reliability concerns such as BTI, HCI, TDDB, and self-heating are addressed via material and process co-optimization.

Finally, I will discuss the roadmap toward 3-D integration, Complementary FETs (CFETs), and Back Side Power Delivery Networks (BSPDN), outlining paths toward sub-1 nm logic in the angstrom era.

Fellow and Professor

Dr. Dong-Won Kim

SAMSUNG

Dr. Dong-Won Kim is a Fellow and Professor at the Samsung Semiconductor Institute of Technology (SSIT). He previously led logic-device development for the 2 nm and beyond technology nodes as a Fellow in the Logic Technology Development group of the Samsung Semiconductor R&D Center. His research has consistently been at the forefront of semiconductor innovation, spanning nano-scaled devices, 3-D and 1-D CMOS transistors, and the production of 20 nm, 14 nm, 10 nm, 7 nm, 3 nm, and 2 nm nodes for SoC applications.

Dr. Kim has authored or co-authored more than 124 publications on nano-scale CMOS devices, FinFETs, and gate-all-around (GAA) technologies, including the Multi-Bridge-Channel FET (MBCFET). His pioneering contributions were instrumental in advancing GAA MBCFET research and driving its successful commercialization in advanced logic products. He holds more than 123 U.S. patents, including the original GAA MBCFET patent.

Current research interests at SSIT focus on 3-D stacked FETs, new channel materials, and GAA MBCFET with backside engineering for next-generation logic technologies. In addition, Dr. Kim is authoring a forthcoming chapter titled "Developments of GAAFET Technologies and Future Challenges" for the upcoming book The FET Centennial: Celebrating the Field-Effect Transistor, scheduled for publication in the first half of 2026.

Dr. Kim has served on several IEEE conference technical committees, such as SOI, SNW, VLSI-TSA, IEDM, and ICICDT. He received his B.S. and M.S. degrees from Korea University (Seoul, 1987 & 1997) and his Ph.D. from the University of Texas at Austin (2003).

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Challenges Driving Microelectronics for the Next Decade

First some general market trends and forecasts are highlighted before reviewing advanced CMOS devices such as nanosheets, Forksheets and CFETs and their importance in semiconductor roadmaps. These evolutions imply technological challenges, including the question of the future role of 2D materials. The heterogenous integration of Ge and III-V technologies on a silicon platform enables the on-chip integration of building blocks with different functionality. In recent years there was also a commercial breakthrough of GaN and SiC devices.

High performance computing & AI, consumer electronics (e.g. gaming, AR/VR sets), telecommunications, edge computing, automotives are examples driving the use of chiplets to reduce the overall cost, improve the yield and enhance the reliability of systems. Some challenges, benefits are drawback will be reported. Additionally, very promising results are also obtained for monolithic sequential 3D (S3D) processing based on the processing of different tiers on top of each other. Sequential integration is a strong enabler for SOCs. Backside Power Delivery Networks play an important role. Major trends in above mentioned process integration approaches are reviewed and technological challenges of some process modules and device structures highlighted.

Professor

Prof. Cor Claeys

Cor Claeys was with imec, Leuven, Belgium from 1984 till 2016 and since 1990 Professor at the KU Leuven. His main interests are semiconductor technology, device physics, low frequency noise phenomena, radiation effects and defect engineering. He teaches several short courses in different parts of the world.

He co-edited books on “Low Temperature Electronics” and “Germanium-Based Technologies: From Materials to Devices” and wrote monographs on “Radiation Effects in Advanced Semiconductor Materials and Devices”, “Fundamental and Technological Aspects of Extended Defects in Germanium”, “Random Telegraph Signals in Semiconductor Devices” and “Metals in Silicon- and Germanium-Based Technologies: Origin, Characterization, Control and Electrical Impact”.

He (co)authored 16 book chapters, over 1200 conference presentations and more than 1400 technical papers. He is editor/co-editor of 70 Conference Proceedings. Prof. Claeys is a Fellow of the Electrochemical Society and of IEEE. He was EDS President in 2008-2009 and Division Director on the IEEE Board of Directors in 2012-2013. He is a recipient of the IEEE Third Millennium Medal and received the IEEE EDS Distinguished Service Award

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Thin Film Transistor Technology: From Development History to Future Trend

Thin-film transistors (TFTs) are field-effect devices first proposed by Lilienfeld in 1925. Initially envisioned for circuit applications, TFTs were soon eclipsed by single-crystal Si MOSFET technology. Renewed interest arose when researchers recognized their distinctive advantages—namely substrate versatility and scalability—which led to their adoption in liquid-crystal displays (LCDs). This breakthrough stimulated the development of other TFT-array-based flat-panel displays, including OLED and micro-LED technologies, now ubiquitous in modern electronic products.

Today, the TFT-based flat-panel-display industry ranks as the second-largest sector of electronics, surpassed only by ICs. Large-area products illustrate this maturity: 100-inch TFT-LCD televisions are commercially available for US$1,499. More than two-thirds of current displays rely on amorphous-silicon (a-Si:H) TFTs, whose field-effect mobility is typically below 1 cm²/V·s. To meet performance demands, higher-mobility devices based on poly-Si and oxide semiconductors have been introduced for advanced displays, imaging systems, and ICs. Beyond displays, TFT-based sensors for chemical, physical, and biological detection have been demonstrated, and new applications continue to emerge.

This talk reviews the evolution of TFT technology and outlines future trends. Opportunities include low-cost multifunctional displays of all sizes, high-performance circuits for artificial intelligence and next-generation memory, and flexible electronics for humans and robots. Owing to low processing temperatures and freedom in substrate choice and size, TFTs hold strong promise for biomedical devices and advanced human-interface technologies.

Prof. Yue Kuo

國立陽明交通大學
NATIONAL YANG MING CHIAO TUNG UNIVERSITY

Life Chair Professor

Yue Kuo is a Life Chair Professor, Photonics Department, Life Chair Professor. He is also Emeritus Professor, Texas A&M University. He received Dr. Eng. Sci. and MS from Columbia University and BS from National Taiwan University. He spent 20 years in industry, i.e., the Semiconductor Division of Data General in Silicon Valley and IBM T. J. Watson Research at Yorktown Heights, before joining Texas A&M University in 1998. His honors include Fellow of IEEE, ECS, AVS, MRS, and NAI, IEEE J. J. Ebers Award, SID Special Recognition Award, ECS Edward G. Acheson Award, Gordon E. Moore Medal, etc. He was ECS President in 2018-2019. His research focuses on elucidating the complex relationship between semiconductor devices, materials, and fabrication processes.

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