

<b>Day 0: 1 March 2026, Sunday (Short Courses and Tutorials)</b>			
<b>Venue</b>	<b>Function Room 8 Ground Mezzanine</b>	<b>Function Room 7 Ground Mezzanine</b>	<b>Function Room 6 Ground Mezzanine</b>
<b>08.00 - 08.30</b>	<b>Registration</b>		
	<b>Short Course 1: Semiconductor Advanced Manufacturing Technology</b>	<b>Short Course 2: Semiconductor Design - Modeling: Design Service: Modelling, CAD - Design</b>	<b>Short Course 3: Semiconductor Advanced Reliability and Testing</b>
<b>09.00 - 10.30</b>	<b>Material Innovations and Process Technology Advances to Enable New Device Architectures for Advanced Nodes Below 3nm</b> Srinivas Guggilla <i>Senior Director, Technology Development</i> Applied Materials	<b>A Practical Guide to Design- Technology-Co-Optimization</b> Oskar Baumgartner COO Global TCAD Solutions	<b>Advanced Packaging, Semiconductor and Silicon Photonics Test</b> Clark Liu <i>Chief Technical Marketing Officer</i> Taiwan MJC Co. Ltd
<b>10.30 - 11.00</b>	<b>Break @ Ground Mezzanine</b>		
<b>11.00 - 12.30</b>	<b>Accelerating the AI Era through Heterogeneous Integration</b> Ashok Muthukumaran <i>Senior Director</i> Applied Materials	<b>Accelerating Semiconductor Innovation with AI-Powered FTCO</b> Tao Sun <i>Regional Application Manager</i> Silvaco	<b>A First Step in Ensuring Chiplet Reliability</b> Cher Ming Tan <i>Professor</i> Chang Gung University
<b>12.30 - 13.30</b>	<b>Lunch @ Ground Mezzanine</b>		
	<b>Tutorial 1: Quantum Computing Technologies</b>	<b>Tutorial 2: Artificial Intelligence Devices (Edge Computing)</b>	<b>Tutorial 3: MEMS / Sensors</b>
<b>13.30 - 15.00</b>	<b>Silicon Gate-Defined Quantum Dots for Quantum Computing</b> Ross Leon <i>Staff Quantum Engineer</i> Quantum Motion Technologies	<b>Artificial Intelligence in Semiconductor Test Engineering with Predictive Defect Capability</b> Muthuramu Gurusamy <i>Associate Vice President</i> Tessolve Semiconductor	<b>Emerging Technologies and monolithic solutions: CMOS, MEMS &amp; Sensors, Photonics and Hybrid Integration Paradigm Change</b> Eloi Marigo <i>Senior Manager, SilTerra</i>
<b>15.00 - 15.30</b>	<b>Break @ Ground Mezzanine</b>		
	<b>Tutorial 4: Memory</b>	<b>Tutorial 5: Emerging RF Wireless</b>	<b>Tutorial 6: 2D Transistors</b>
<b>15.30 - 17.00</b>	<b>Spintronic Memristors for Computing</b> Qiming Shao <i>Associate Professor</i> The Hong Kong University of Science and Technology	<b>Emerging RF Materials for Next Generation Wireless Connectivity Circuits and Devices</b> Luis Andia <i>Business Development Director</i> Soitec Microelectronics	<b>From Atoms to Circuits: 2D Materials for Logic Scaling and Monolithic 3D Integration</b> Saptashi Das <i>Ackley Professor of Engineering and MRI Fellow</i> The Pennsylvania State University

<b>Day 1: 2 March 2026, Monday (Conference)</b>			
<b>08.00 - 08:30</b>	<b>Registration</b>		
<b>08:30 - 09:00</b>	<b>Opening Ceremony @ Ballroom 3, Lower Ground Floor</b>		
<b>09:00 - 09:45</b>	<b>Plenary 1: The Future of Memory Chip Technology and Role of Innovation</b> Gurtej Sandhu <i>Principal Fellow and Corporate Vice President, Micron Technology</i>		
<b>09:45 - 10:30</b>	<b>Plenary 2: Critical Technologies for Chiplet Integration</b> Subramaniam Iyer <i>Distinguished Professor, University of California, Los Angeles</i>		
<b>10:30 - 10:45</b>	<b>Advancing Technology Together: Inside IEEE EDS Publications</b> Renuka P. Jindal <i>Associate Vice-President, EDS Publications and Products</i>		
<b>10:45 - 11:00</b>	<b>Break + Exhibition @ Grand Foyer, Lower Ground Floor</b>		
<b>11.00 - 11.45</b>	<b>Keynote 1: AI in Every Layer: Enabling Velocity and Time to Solution</b> David Fried <i>Corporate Vice President, Lam Research</i>		
<b>11.45 - 12.30</b>	<b>Keynote 2: Powering AI Today and Tomorrow</b> Chee How Tan <i>Vice President, Infineon</i>		
<b>12:30 - 13:30</b>	<b>Lunch @ Ballroom 2, Lower Ground Floor</b> <b>Poster Session 1 @ Grand Foyer, Lower Ground Floor</b>		
<b>13:30 - 15:10</b>	<table border="0" style="width: 100%;"> <tr> <td style="width: 50%; text-align: center;"> <b>Technical Parallel Session #1</b>            @ Function Rooms 3 to 12            Lower Ground Floor and Ground Mezzanine Floor         </td> <td style="width: 50%; text-align: center;"> <b>Industry Panel Session</b>            @ Function Room 1, Lower Ground Floor         </td> </tr> </table>	<b>Technical Parallel Session #1</b> @ Function Rooms 3 to 12 Lower Ground Floor and Ground Mezzanine Floor	<b>Industry Panel Session</b> @ Function Room 1, Lower Ground Floor
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<b>15:10 - 15:25</b>	<b>Break + Exhibition @ Grand Foyer, Lower Ground Floor</b>		
<b>15:25 - 18:25</b>	<b>Special Session I: FET100 Forum @ Ballroom 3, Lower Ground Floor</b> Hiroshi Iwai, <i>Distinguished Chair Professor, National Yang Ming Chiao Tung University</i> Dong-Won Kim, <i>Fellow, Samsung Electronics</i> Cor Claeys, <i>Distinguished Professor, KU Leuven</i> Yue Kuo, <i>Life Chair Professor, National Yang Ming Chiao Tung University</i>		
<b>18:25 - 19:30</b>	<b>Special Session II: Women in Electron Devices / Young Professionals Panel Session</b> Beth Yam, <i>Senior Director, Intel</i> Gauri Karve, <i>Scientific Director, IMEC</i> Eu Poh Leng, <i>Senior Director, NXP Semiconductors</i> Avinash Kumar, <i>Chair, IEEE EDS UKM Student Branch</i>		
<b>19:30 - 21:00</b>	<b>Welcome Reception @ Ballroom 4, Lower Ground Floor</b>		

Day 2: 3 March 2026, Tuesday (Conference)			
09.00 - 09:45	<b>Plenary 3: Manufacturing the Next Era: AI, Remote Operations &amp; the Future of Semiconductor Innovation</b> Yvonne Keil <i>Senior Director, GlobalFoundries</i>		
09:45 - 10:30	<b>Keynote 3: Traces of Device and Computer Evolution — From Concept to Computer to Artificial Intelligence</b> Digh Hisamoto <i>Chief Senior Scientist, Hitachi Ltd</i>		
10.30 - 10:45	<b>Break + Exhibition @ Grand Foyer, Lower Ground Floor</b>		
10.45 - 11.30	<b>Keynote 4: From Talent to Silicon: Accelerating Malaysia's Sustainable Advanced Semiconductor Ecosystem</b> Abdul Rahman Mohamed <i>Vice Chancellor, Universiti Sains Malaysia</i>		
11.30 - 12.15	<b>Keynote 5: National Agenda on Bridging Semiconductor and Quantum Technology</b> Sufian Jusoh <i>Vice-Chancellor, Universiti Kebangsaan Malaysia</i>		
12:15 - 12:30	<b>Building Malaysia's Complete Silicon Ecosystem</b> Angel Low <i>General Manager, ASEM under Malaysia IC Design Park</i>		
12:30 - 13:15	<b>Lunch @ Ballroom 2, Lower Ground Floor</b> <b>Poster Session 2 @ Grand Foyer, Lower Ground Floor</b>		
13:15 - 15:15	<b>Special Session III: Industry Panel Session</b>		
15:15 - 16:55	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%; text-align: center; vertical-align: top;"> <b>Technical Parallel Session #2</b>            @ Function Rooms 3 to 12            Lower Ground Floor and Ground Mezzanine Floor         </td> <td style="width: 40%; text-align: center; vertical-align: top;"> <b>13:30 - 16:30</b>  <b>Ethical AI For Innovation &amp; Decision Confidence</b>            @ Function Room 1, Lower Ground Floor         </td> </tr> </table>	<b>Technical Parallel Session #2</b> @ Function Rooms 3 to 12 Lower Ground Floor and Ground Mezzanine Floor	<b>13:30 - 16:30</b> <b>Ethical AI For Innovation &amp; Decision Confidence</b> @ Function Room 1, Lower Ground Floor
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16:55 - 17:10	<b>Break @ Lower Ground Floor and Ground Mezzanine Floor</b>		
17:10 - 19:30	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%; text-align: center; vertical-align: top;"> <b>Technical Parallel Session #3</b>            @ Function Rooms 3 to 12            Lower Ground Floor and Ground Mezzanine Floor         </td> <td style="width: 40%; text-align: center; vertical-align: top;"> <b>Focus Session: Focus Session: Bio-Hybrid Electronics</b>            @ Function Room 1, Lower Gound Floor         </td> </tr> </table>	<b>Technical Parallel Session #3</b> @ Function Rooms 3 to 12 Lower Ground Floor and Ground Mezzanine Floor	<b>Focus Session: Focus Session: Bio-Hybrid Electronics</b> @ Function Room 1, Lower Gound Floor
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19:30 - 21:30	<b>Banquet @ Ballroom 3, Lower Ground Floor</b>		

<b>Day 3: 4 March 2026, Wednesday (Conference)</b>	
<b>08:30 - 09:15</b>	<b>Plenary 4: Shaping the Next Era of Semiconductor Innovation: From AI-Driven Devices to Advanced Manufacturing</b> Kazunari Ishimaru <i>CTO, Rapidus</i>
<b>09:15 - 10:00</b>	<b>Plenary 5: Ultra-clean Interfaces in Atomically Thin Materials for Electronics</b> Manish Chhowalla <i>Goldsmiths' Professor, University of Cambridge</i>
<b>10:00 - 10:15</b>	<b>Defect Localization and Atomic-Scale Root-Cause Analysis by Using Cs-Corrected Electron Optics and Triple Beam System for High-Definition Lamella Preparation</b> Abby Soo <i>Technical PA, Hi-Tech Instruments</i>
<b>10:15 - 10:30</b>	<b>Break + Exhibition @ Grand Foyer, Lower Ground Floor</b>
<b>10:30 - 11:15</b>	<b>Keynote 6: Superconducting Qubit Design and Integration: Relationship to the Semiconductor Industry</b> Hiu-Yung Wong <i>Distinguished Professor, San Jose State University</i>
<b>11:15 - 12:00</b>	<b>Keynote 7: The Opportunity of 3D Resistive-gate to Replace Floating Gate Memory in the Angstrom Generation</b> Steve Chung Shao-Shiun <i>Lifetime Chair Professor, National Yang Ming Chiao Tung University</i>
<b>12:00 - 12:45</b>	<b>Keynote 8: Intelligent Infrared Photodetectors</b> Weida Hu <i>Vice President, Shanghai Institute of Technical Physics, Chinese Academy of Sciences</i>
<b>12:45 - 13:45</b>	<b>Lunch @ Ballroom 2, Lower Ground Floor</b> <b>Poster Session 2 @ Grand Foyer, Lower Ground Floor</b>
<b>13:45 - 16:15</b>	<b>Technical Parallel Session #4</b> @ Function Rooms 3 to 12 Lower Ground Floor and Ground Mezzanine Floor
<b>16:15 - 16:30</b>	<b>Break + Exhibition @ Grand Foyer, Lower Ground Floor</b>
<b>16:30 - 17:00</b>	<b>Award Presentation and Closing Ceremony @ Ballroom 3, Lower Ground Floor</b>

<b>Day 4: 5 March 2026, Thursday (Industry Visit)</b>			
	<b>Tour 1: SilTerra + MIMOS</b> Time: 08:00 - 14:30	<b>Tour 2: ams OSRAM</b> Time: 08:30 - 12:30	<b>Tour 3: Inari Amertron</b> Time: 09:30 - 12:30